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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: DALE E. GULICK	Group Art Unit: 2137
Serial No.: 10/084,596	Examiner: J. Williams
Filed: FEBRUARY 27, 2002	Atty. Dkt. No.: 2000.051900
For: EMBEDDED PROCESSOR WITH DIRECT CONNECTION OF SECURITY DEVICES FOR ENHANCED SECURITY	

DECLARATION UNDER 37 C.F.R. § 1.131 OF DALE E. GULICK

1. My name is Dale E. Gulick. I have personal knowledge of the facts stated herein.

2. I am currently employed with Advanced Micro Devices, Inc. in Austin, Texas. I am a named inventor on application Serial No. 10/084,596 entitled "Embedded Processor with Direct Connection of Security Devices for Enhanced Security."

3. Attached as Exhibit A is a copy of the invention disclosure form I prepared in Austin, Texas for the invention described in the above-referenced patent application. I prepared and signed the invention disclosure form on January 28, 2000, as indicated by the date adjacent my signature.

4. The attached invention disclosure form was provided with internal tracking number TT4033 by AMD's legal department, and it was sent to the law firm of Williams, Morgan & Amerson on or about May 12, 2000, with a request to prepare a United States patent application for the invention disclosed in the invention form.

EXHIBIT
A

5. I understand that willful false statements and the like so made are punishable by fine or imprisonment, or both, and may jeopardize the validity of the application or any patent issuing thereon.

6. I declare under penalty of perjury that the foregoing is true and correct.

1/6/06
Date

Dale E. Gulick

AMD
5204 E. Ben White Blvd.
Austin, TX 78741
Tel (512) 385-8542

12MY2000

J. MIKE AMERSON
WILLIAMS, MORGAN & AMERSON
7676 HILLMONT, SUITE 250
HOUSTON, TX 77040

2000.051900

RE: Invention Disclosure TT4033

Entitled:
PC SYSTEM WITH AN EMBEDDED PROCESSOR WITH DIRECT CONNECTION OF SECURITY DEVICES TO THE EMBEDDED PROCESSOR FOR ENHANCED

Dear J. MIKE AMERSON:

Please prepare a US patent application for the subject invention disclosureand file the application in the USPTO within two months of this letter. A copy of theInvention Disclosure is enclosed.

Please follow the instructions set forth in AMD's DIRECTIONS TO OUTSIDE COUNSEL REGARDING PREPARATION AND PROSECUTION OF PATENT APPLICATIONS Version 1.0 dated May 1, 1996.

It is not necessary to prepare a PCT international application at this time. If one is later determined to be needed, AMD will so advise you.

If you have any questions or need additional information, please call me at 512-602-5964, or the responsible AMD Technology Law attorney, LOUIS A. RILEY at 512-602-2788.

Sincerely,

Samantha Cardona
Paralegal
Technology Law Department

Enclosure

cc:
GULICK, DALE E. 61682 (TX)

INVENTION DISCLOSURE AMD CONFIDENTIAL

Legal Dept. Use: ID# TT 1033

Received _____

In Texas:
Return to M/S 562
Call x55964 for assistance

In California:
Return to M/S 68
Call x26542 for assistance

INVENTION IDENTIFICATION:

WORKING TITLE: PC SYSTEM WITH AN EMBEDDED PROCESSOR WITH DIRECT CONNECTION OF SECURITY DEVICES TO THE EMBEDDED PROCESSOR FOR ENHANCED SECURITY

BRIEF DESCRIPTION AND/OR SKETCH OF INVENTION (you may submit copies of Engineering Notebook pages, reports or drawings as ATTACHMENTS and describe below):

SEE ATTACHED

Engineering Notebook No. _____ Page Numbers: _____ Number of Drawings _____

ADVANTAGES (Check all that apply):

_____ Lower Cost	_____ Improves Linearity
_____ Simplifies Manufacturing	_____ Improves Accuracy
_____ Fewer Parts	_____ Higher Operating Speeds
_____ Simpler Construction	_____ Improves Signal -to -Noise Ratio
_____ New Function	_____ Improves Efficiency
_____ Improves Reliability	_____ Improves Wear Characteristics
✓ New Technology	_____ Designs Around Existing Patent
_____ Solves the following problem(s) _____	

_____ Other Advantages _____

GENERAL INFORMATION:

TECHNOLOGY to which the invention relates PC CHIPSETS

AMD PRODUCT or PROJECT NAME invention would be used in (if any) ZORAK

Government Dept (Army, Air Force, etc.) and Contract No. _____

PLEASE ESTIMATE:

Cost per unit $ 10

Sales potential $ 500M per 5 years

Product life (Number of years) 10 - DEFINITIVE 5

Product/Process No. _____

LIST DATES OF:

First written description of invention / /
First Drawing / /
First Oral Disclosure / / Disclosed to (name) _____
First Disclosure (i.e. product announcement, external presentation, sampling, offer for sale, etc.) / / Specify _____
Non-Disclosure Agreement: / /
Device First Completed: / /
First Successful Test: / / Made by (Name) _____ Tested by (Name)_____
Prototype Location: _____
First Published: / / Publication Name: _____
Introduction of product using invention / /

INVENTOR INFORMATION:

Inventor Signature and Date Dale E Gulick 1/26/06
Inventor's Printed Name DALE GULICK
Employee #61682 Extension 5702 Home Telephone 263-7693 Citizenship USA
Home Address 11715 ASTORIA DR AUSTIN TX 78733
Mailstop 535 Dept # 7952 Division Name PPD Supervisor Name HERE VP Name HERE

Co-Inventor Signature and Date _____
Co-Inventor's Printed Name _____
Employee #_____ Extension _____ Home Telephone _____ Citizenship _____
Home Address _____
Mailstop ___ Dept # _____ Division Name ____ Supervisor Name _____ VP Name _____

Co-Inventor Signature and Date _____
Co-Inventor's Printed Name _____
Employee #_____ Extension _____ Home Telephone _____ Citizenship _____
Home Address _____
Mailstop ___ Dept # _____ Division Name ____ Supervisor Name _____ VP Name _____

If there are additional co-inventors, list on separate sheet and check here ☐

WITNESSED BY:

I have read and understood this disclosure and read and signed each page of the attachments:
Witness 1 Signature _____ Date _____
Printed Name and Employee # _____
Witness 2 Signature _____ Date _____
Printed Name and Employee # _____

PATENT DEPARTMENT USE ONLY

I have reviewed and understood this Invention Disclosure, and it (is) (is not) recommended to AMD for review for patenting at this time. It should be given (high) (normal) (low) priority.
BY (Signature) _____ Date _____
PRINT NAME _____ Employee Number _____

Autonomous Management Processor (AMP) – IP

1) An IOH with an embedded ASF engine
   a) Supports both master and slave mode
   b) 8051-based ASF engine in the IOH (not on the NIC)

2) Basic embedded 8051 architecture
   a) IOH with embedded controller
   b) Connection to an integrated Ethernet core
   c) Modifications to the Ethernet core to route ASF messages to the ASF buffers
   d) x86 -> 8051 communications structure, including interrupts
   e) 8051 -> x86 communications structure, including interrupts
   f) P&P configuration space for ASF
   g) 8051 code stored in on-chip ROM, and shadowed from BIOS ROM into on-chip RAM – also running directly out of BIOS ROM
   h) 8051/IOH control of system RESET and power supply based on RMCP commands
   I) Resources in RTC well, 8051 in suspend well

3) Use of the AMP for both ASF and ACPI functions
   a) embedding a controller in the chipset that is ACPI chapter 13 compliant
   b) Using the AMP for both functions
   c) System with both general x86 -> 8051 interface and a chapter 13 compliant interface
   d) 8051 calling SMI-based x86 routines

4) Watchdog Timer/ASF system state determination (interpreting WDT timeouts in the context of system status (various BIOS boot states, etc.)

5) Hardware interlock that prevents an RMCP Reset or power down or power cycle from happening when the CPU is not hung. Needs to be a write-once initialization option. Tied into the WDT.

6) Hanging a smart card reader off of the AMP. Also biometric input devices.

7) SMI trap on reset and power down commands. Receipt of the command causes an SMI with a vector in the SEM trap register. The SMI code executes the command if it determines it to be valid. It also sets a timer = 1 second +1second, -0.001. If the timer expires before being reset by the SMI code – reset can only happen from within SMM – the command is executed by the AMP hardware.

8) 8051 code structure
   a) Master control loop
   b) Polling task
   c) SMBus emulation task
   d) ASF slave mode support
   e) Incoming Push mode sensor messages on the SMBus
   f) Address Resolution Protocol
   g) Packet construction/decomposition

9) Embedded controller firmware structure with a hardware errant task termination mechanism
   a) Hardware timer
   b) All tasks having a clean-up and exit call
   c) Makes errant tasks non-fatal
   d) Task ID and sequence number